CLAIMS

1. A field effect transistor comprising:

a semiconductor layer projecting upward from the plane of a base;

a gate electrode provided on opposite side surfaces of the semiconductor layer;

a gate insulating film interposed between the gate electrode and the side surface of said semiconductor layer; and

source/drain regions where a first conductivity type impurity is introduced in said semiconductor layer,

wherein said semiconductor layer has a channel forming region in a portion sandwiched between said source/drain regions, and has on the upper part of the semiconductor layer in the channel forming region a channel impurity concentration adjusting region of which the concentration of a second conductivity type impurity is higher than that of the lower part of the semiconductor layer, and

in the channel impurity concentration adjusting region, a channel is formed on a side surface portion of the semiconductor layer in the channel impurity concentration adjusting region, which faces said gate insulating film, in a state of operation in which a signal voltage is applied to said gate electrode.

2. A field effect transistor comprising:

a semiconductor layer projecting upward from the plane of a base;

a gate electrode extending from the upper part of the semiconductor layer to facing opposite side surfaces so as to straddle the semiconductor layer;

a gate insulating film interposed between the gate electrode and said semiconductor layer; and

source/drain regions where a first conductivity type impurity is introduced in said semiconductor layer,

wherein said semiconductor layer has a channel forming region in a portion sandwiched between said source/drain regions, and has on the upper part of the semiconductor layer in the channel forming region a channel impurity concentration adjusting region of which the concentration of a second conductivity type impurity is higher than that of the lower part of the semiconductor layer, and

in the channel impurity concentration adjusting region, a channel is formed on upper surface and side surface portions of the semiconductor layer in the channel impurity concentration adjusting region, which face said gate insulating film, in a state of operation in which a signal voltage is applied to said gate electrode.

3. The field effect transistor according to claim 1 or 2, wherein when having in the upper part of the semiconductor layer a concentration of the second conductivity type impurity which is same as that in the lower part of the semiconductor layer, said channel impurity concentration adjusting region has an impurity concentration with which

an electric potential increasing in a corner portion of the upper part of the semiconductor layer can be reduced for an n-channel transistor; and

a reduction in electric potential in the corner portion of the upper part of the semiconductor layer can be downscaled for a p-channel transistor.

4. The field effect transistor according to claim 1, 2 or 3, wherein the filed effect transistor has an impurity concentration with which

an electric potential increasing in the corner portion of the upper part of the semiconductor layer can be reduced by 60 mV or more for the n-channel transistor; and

a reduction in electric potential in the corner portion of the upper part of the semiconductor layer can be downscaled by 60 mV or more for the p-channel transistor.

5. The field effect transistor according to any one of claims 1 to 4, wherein the average value of the net concentration of the second conductivity type impurity in said channel impurity concentration adjusting region is in a range from 1.3 times or more to 4 times or less as large as the average value of the net concentration of the second conductivity type impurity in other regions below the channel impurity concentration adjusting region.

6. The field effect transistor according to any one of claims 1 to 4, wherein the average value of the net concentration of the second conductivity type impurity in said channel impurity concentration adjusting region is in a range from 1.5 times or more to 3 times or less as large as the average value of the net concentration of the second conductivity type impurity in other regions below the channel impurity concentration adjusting region.

7. The field effect transistor according to any one of claims 1 to 6, wherein in said channel impurity concentration adjusting region, a depth Htop extending downward from the upper end of said semiconductor layer is 0.7 times or less as large as a width Wfin of the semiconductor layer parallel to the plane of the base and vertical to the longitudinal direction of the channel.

8. The field effect transistor according to any one of claims 1 to 7, wherein in said channel impurity concentration adjusting region, a depth Htop extending downward from the upper end of said semiconductor layer is 7/40 times or more as large as a width Wfin of the semiconductor layer parallel to the plane of the base and vertical to the longitudinal direction of the channel.

9. The field effect transistor according to any one of claims 1 to 8, wherein in said channel impurity concentration adjusting region, the depth Htop extending downward from the upper end of said semiconductor layer is in a range from 5 to 24.5 nm.

10. The field effect transistor according to any one of claims 1 to 9, wherein the average value of the net concentration of the second conductivity type impurity in said channel forming region excepting said channel impurity concentration adjusting region is 1×10^{18} cm^{-3} or more.

11. The field effect transistor according to any one of claims 1 to 10, wherein said channel impurity concentration adjusting region is provided along an entire in-plane direction parallel to the plane of the base in the upper part of the semiconductor layer in said channel forming region.

12. The field effect transistor according to any one of claims 1 to 10, wherein the field effect transistor has as said channel impurity concentration adjusting region the channel impurity concentration adjusting region so as to include at least a part of the corner portion of the semiconductor layer, in the upper part of the semiconductor layer in said channel forming region, and further has a portion which does not have the channel impurity concentration adjusting

region in a section parallel to the plane of the base, which includes the channel impurity concentration adjusting region.

13. The field effect transistor according to claim 12, wherein the field effect transistor has a first channel impurity concentration adjusting region provided seamlessly along the longitudinal direction of the channel so as to include one corner portion and establish a link between a pair of source/drain regions and a second channel impurity concentration adjusting region provided seamlessly along the longitudinal direction of the channel so as to include the other corner portion and establish a link between a pair of source/drain regions, in the upper part of the semiconductor layer in said channel forming region, and further has between the first channel impurity concentration adjusting region and the second channel impurity concentration adjusting region a portion which does not have these channel impurity concentration adjusting regions over an area between a pair of source/drain regions so that these channel impurity concentration adjusting regions are mutually separated.

14. The field effect transistor according to claim 12, wherein the field effect transistor has a first channel impurity concentration adjusting region provided seamlessly from one corner portion to the other corner portion so as to contact one source/drain region and a second channel impurity concentration adjusting region provided seamlessly from one corner to the other corner so as to contact the other source/drain region, in the upper part of the semiconductor layer in said channel forming region, and further has between the first channel impurity concentration adjusting region and the second channel impurity concentration adjusting region a portion which does not have these channel impurity concentration adjusting regions over an area between a pair of corner portions

so that these channel impurity concentration adjusting regions are mutually separated.

15. The field effect transistor according to claim 12, wherein the field effect transistor has a channel impurity concentration adjusting region provided seamlessly from one corner portion to the other corner portion so as to contact one source/drain region, in the upper part of the semiconductor layer in said channel forming region, and has no channel impurity concentration adjusting region between said channel impurity concentration adjusting region and the other source/drain region.

16. The field effect transistor according to claim 12, wherein the field effect transistor has a first channel impurity concentration adjusting region contacting one source/drain region and including a part of a first corner portion, a second impurity concentration adjusting region contacting the other source/drain region and including a part of the first corner portion, a third channel impurity concentration adjusting region contacting one source/drain region and including a part of a second corner portion facing the first corner portion, and a fourth channel impurity concentration adjusting region contacting the other source/drain region and including a part of the second corner portion facing the first corner portion, in the upper part of the semiconductor layer in said channel forming region, and further has a portion which does not have these channel impurity concentration adjusting regions over an area between a pair of source/drain regions and an area between a pair of first/second corner portions so that these channel impurity concentration adjusting regions are mutually separated.

17. The field effect transistor according to claim 12, wherein the field effect transistor has a first channel impurity concentration adjusting region contacting a first source/drain region and including a part of a first corner portion and a second channel impurity concentration adjusting region contacting said first source/drain region and including a part of a second corner portion facing the first corner portion, in the upper part of the semiconductor layer in said channel forming region,

has a portion having no channel impurity concentration adjusting region between said first channel impurity concentration adjusting region and said second channel impurity concentration adjusting region, and

has no channel impurity concentration adjusting region in the vicinity of a second source/drain region facing the first source/drain region.

18. A field effect transistor having an impurity concentration comprising:

a semiconductor layer projecting upward from the plane of a base;

a gate electrode provided on opposite side surfaces of the semiconductor layer;

a gate insulating film interposed between the gate electrode and the side surface of said semiconductor layer; and

source/drain regions where a first conductivity type impurity is introduced in said semiconductor layer,

wherein said semiconductor layer has a channel forming region in a portion sandwiched between said source/drain regions, has in the upper part of the semiconductor layer in the portion sandwiched between the source/drain regions a channel impurity concentration adjusting region of which the concentration of a second conductivity type impurity is higher than that in the lower part of the semiconductor layer, so as to include at least a part of a

corner portion of the semiconductor layer, and further has a portion which does not have the channel impurity concentration adjusting region in a section parallel to the plane of the base, which includes the channel impurity concentration adjusting region.

19. A field effect transistor having an impurity concentration comprising:

a semiconductor layer projecting upward from the plane of a base;

a gate electrode extending from the upper part of the semiconductor layer to facing opposite side surfaces so as to straddle the semiconductor layer;

a gate insulating film interposed between the gate electrode and said semiconductor layer; and

source/drain regions where a first conductivity type impurity in said semiconductor layer,

wherein said semiconductor layer has a channel forming region in a portion sandwiched between said source/drain regions, has in the upper part of the semiconductor layer in the portion sandwiched between the source/drain regions a channel impurity concentration adjusting region of which the concentration of a second conductivity type impurity is higher than that in the lower part of the semiconductor layer, so as to include at least a part of a corner portion of the semiconductor layer, and further has a portion which does not have the channel impurity concentration adjusting region in a section parallel to the plane of the base, which includes the channel impurity concentration adjusting region.

20. The field effect transistor according to claim 18 or 19, wherein the field effect transistor has a first channel impurity concentration adjusting region

provided seamlessly along the longitudinal direction of a channel so as to include one corner portion and establish a link between a pair of source/drain regions and a second channel impurity concentration adjusting region provided seamlessly along the longitudinal direction of the channel so as to include the other corner portion and establish a link between a pair of source/drain regions, in the upper part of the semiconductor layer in the portion sandwiched between said source/drain regions, and further has between the first channel impurity concentration adjusting region and the second channel impurity concentration adjusting region a portion which does not have these channel impurity concentration adjusting regions over an area between a pair of source/drain regions so that these channel impurity concentration adjusting regions are mutually separated.

21. The field effect transistor according to claim 18 or 19, wherein the field effect transistor has a first channel impurity concentration adjusting region provided seamlessly from one corner portion to the other corner portion so as to contact one source/drain region and second channel impurity concentration adjusting region provided seamlessly from one corner portion to the other corner portion so as to contact the other source/drain region, in the upper part of the semiconductor layer in the portion sandwiched between said source/drain regions, and further has between the first channel impurity concentration adjusting region and the second channel impurity concentration adjusting region a portion which does not have these channel impurity concentration adjusting regions over an area between a pair of corner portions so that these channel impurity concentration adjusting regions are mutually separated.

22. The field effect transistor according to claim 18 or 19, wherein the field effect transistor has a channel impurity concentration adjusting region provided seamlessly from one corner portion to the other corner portion so as to contact one source/drain region in the upper part of the semiconductor layer in the portion sandwiched between said source/drain regions, and

has no channel impurity concentration adjusting region between said channel impurity concentration adjusting region and the other source/drain region.

23. The field effect transistor according to claim 18 or 19, wherein the field effect transistor has a first channel impurity concentration adjusting region contacting one source/drain region and including a part of a first corner portion, a second impurity concentration adjusting region contacting the other source/drain region and including a part of the first corner portion, a third channel impurity concentration adjusting region contacting one source/drain region and including a part of a second corner portion facing the first corner portion, and a fourth channel impurity concentration adjusting region contacting the other source/drain region and including a part of the second corner portion facing the first corner portion, in the upper part of the semiconductor layer in the portion sandwiched between said source/drain regions, and further has a portion which does not have these channel impurity concentration adjusting regions over an area between a pair of source/drain regions and an area between a pair of first/second corner portions so that these channel impurity concentration adjusting regions are mutually separated.

24. The field effect transistor according to claim 18 or 19, wherein the field effect transistor has a first channel impurity concentration adjusting region

contacting a first source/drain region and including a part of a first corner portion and a second channel impurity concentration adjusting region contacting said first source/drain region and including a part of a second corner portion facing the first corner portion, in the upper part of the semiconductor layer in the portion sandwiched between said source/drain regions,

has a portion having no channel impurity concentration adjusting region between said first channel impurity concentration adjusting region and said second channel impurity concentration adjusting region, and

has no channel impurity concentration adjusting region in the vicinity of a second source/drain region facing the first source/drain region.

25. The field effect transistor according to claim 18 or 19, wherein in said channel impurity concentration adjusting region, the average value of the net concentration of the second conductivity type impurity in the channel impurity concentration adjusting region is in a range from 1.3 times or more to 4 times or less as large as the average value of the net concentration of the second conductivity type impurity in other regions below the channel impurity concentration adjusting region, in a section vertical to the plane of the base, which includes the channel impurity concentration adjusting region.

26. The field effect transistor according to claim 18 or 19, wherein in said channel impurity concentration adjusting region, the average value of the net concentration of the second conductivity type impurity in the channel impurity concentration adjusting region is in a range from 1.5 times or more to 3 times or less as large as the average value of the net concentration of the second conductivity type impurity in other regions below the channel impurity

concentration adjusting region, in a section vertical to the plane of the base, which includes the channel impurity concentration adjusting region.

27. The field effect transistor according to claim 18 or 19, wherein said channel impurity concentration adjusting region has a concentration distribution in which the average value of the net concentration of the second conductivity type impurity in the channel impurity concentration adjusting region is in a range from 1.3 times or more to 4 times or less as large as the average value of the net concentration of the second conductivity type impurity in other regions below the channel impurity concentration adjusting region, on a line vertical to the plane of the base in the semiconductor layer in the portion sandwiched between said source/drain regions.

28. The field effect transistor according to claim 18 or 19, wherein said channel impurity concentration adjusting region has a concentration distribution in which the average value of the net concentration of the second conductivity type impurity in the channel impurity concentration adjusting region is in a range from 1.5 times or more to 3 times or less as large as the average value of the net concentration of the second conductivity type impurity in other regions below the channel impurity concentration adjusting region, on a line vertical to the plane of the base in the semiconductor layer in the portion sandwiched between said source/drain regions.

29. The field effect transistor according to any one of claims 18 to 28, wherein in said channel impurity concentration adjusting region, a depth Htop extending downward from the upper end of said semiconductor layer is 0.7

times or less as large as a width Wfin of the semiconductor layer parallel to the plane of the base and vertical to the longitudinal direction of the channel.

30. The field effect transistor according to any one of claims 18 to 28, wherein in said channel impurity concentration adjusting region, a depth Htop extending downward from the upper end of said semiconductor layer is 7/40 times or more as large as a width Wfin of the semiconductor layer parallel to the plane of the base and vertical to the longitudinal direction of the channel.

31. The field effect transistor according to any one of claims 18 to 28, wherein in said channel impurity concentration adjusting region, the depth Htop extending downward from the upper end of said semiconductor layer is in a range from 5 to 24.5 nm.

32. The field effect transistor according to any one of claims 18 to 31, wherein the average value of the net concentration of the second conductivity type impurity in said channel forming region excepting said channel impurity concentration adjusting region is 1×10^{18} cm^{-3} or more.

33. The field effect transistor according to claim 1, 2, 18 or 19, wherein said semiconductor layer has an upper channel impurity concentration adjusting region which is said channel impurity concentration adjusting region provided in the upper part of the semiconductor layer, a middle channel forming region which is provided below the upper channel impurity concentration adjusting region and of which the concentration of the second conductivity type impurity is lower than that in the upper channel impurity concentration adjusting region, and a lower channel impurity concentration adjusting region which is provided

in the lower part of the semiconductor layer below the middle channel forming region and of which the concentration of the second conductivity type impurity is higher than that in the middle channel forming region.

34. The field effect transistor according to claim 33, wherein said lower channel impurity concentration adjusting region has a channel formed in a side surface portion of the semiconductor layer in the lower channel impurity concentration adjusting region, which faces said gate insulating film, in a state of operation in which a signal voltage is applied to said gate electrode.

35. The field effect transistor according to claim 33 or 34, wherein said lower channel impurity concentration adjusting region has an impurity concentration with which an electric potential increasing in the corner portion of the lower part of the semiconductor layer can be reduced when said lower channel impurity concentration adjusting region has a concentration of the second conductivity type impurity which is same as that in said middle channel forming region.

36. The field effect transistor according to claim 33, 34 or 35, wherein the average value of the net concentration of the second conductivity type impurity in said lower channel impurity concentration adjusting region is 1.3 times or more and 4 times or less as large as the average value of the net concentration of the second conductivity type impurity in said middle channel forming region.

37. The field effect transistor according to claim 36, wherein the average value of the net concentration of the second conductivity type impurity in said upper channel impurity concentration adjusting region is 1.3 times or more and

4 times or less as large as the average value of the net concentration of the second conductivity type impurity in said middle channel forming region.

38. The field effect transistor according to claim 33, 34 or 35, wherein the average value of the net concentration of the second conductivity type impurity in said lower channel impurity concentration adjusting region is 1.5 times or more and 3 times or less as large as the average value of the net concentration of the second conductivity type impurity in said middle channel region.

39. The field effect transistor according to claim 38, wherein the average value of the net concentration of the second conductivity type impurity in said upper channel impurity concentration adjusting region is 1.5 times or more and 3 times or less as large as the average value of the net concentration of the second conductivity type impurity in said middle channel forming region.

40. The field effect transistor according to any one of claims 33 to 39, wherein in said lower channel impurity concentration adjusting region, a height Htop2 extending upward from the lower end of said semiconductor layer is 0.7 times or less as large as a width Wfin of said semiconductor layer parallel to the plane of the base and vertical to the longitudinal direction of the channel.

41. The field effect transistor according to claim 40, wherein in said upper channel impurity concentration adjusting region, the height Htop2 extending upward from the lower end of said semiconductor layer is 0.7 times or less as large as the width Wfin of said semiconductor layer parallel to the plane of the base and vertical to the longitudinal direction of the channel.

42. The field effect transistor according to any one of claims 33 to 40, wherein in said lower channel impurity concentration adjusting region, the height Htop2 extending upward from the lower end of said semiconductor layer is 7/40 times or more as large as the width Wfin of the semiconductor layer parallel to the plane of the base and vertical to the longitudinal direction of the channel.

43. The field effect transistor according to claim 42, wherein in said upper channel impurity concentration adjusting region, the height Htop2 extending upward from the lower end of said semiconductor layer is 7/40 times or more as large as a width Wfin of the semiconductor layer parallel to the plane of the base and vertical to the longitudinal direction of the channel.

44. The field effect transistor according to any of claims 33 to 43, wherein in said lower channel impurity concentration adjusting region, the height Htop2 extending upward from the lower end of said semiconductor layer is in a range from 5 to 24.5 nm.

45. The field effect transistor according to claim 44, wherein in said upper channel impurity concentration adjusting region, the height Htop2 extending upward from the lower end of said semiconductor layer is in a range from 5 to 24.5 nm.

46. The field effect transistor according to any one of claims 33 to 45, wherein said lower channel impurity concentration adjusting region is provided along an entire in-plane direction parallel to the plane of the base in the lower

part of the semiconductor layer in the portion sandwiched between source/drain regions.

47. The field effect transistor according to any one of claims 33 to 45, wherein the field effect transistor has as said lower channel impurity concentration adjusting region the channel impurity concentration adjusting region so as to include at least a part of the corner portion of the semiconductor layer in the lower part of the semiconductor layer in the portion sandwiched between said source/drain regions, and further has a portion which does not have the lower channel impurity concentration adjusting region in a section parallel to the plane of the base, which includes the lower channel impurity concentration adjusting region.

48. The field effect transistor according to any one of claims 33 to 47, wherein the average value of the net concentration of the second conductivity type impurity in said channel forming region excepting said upper channel impurity concentration adjusting region and said lower channel impurity concentration adjusting region is 1×10^{18} cm^{-3} or more.

49. The field effect transistor according to claim 1 or 18, wherein a cap insulating film thicker than said gate insulating film is provided between the upper part of said semiconductor layer and said gate electrode so that no channel is formed on the upper surface of the semiconductor layer.

50. The field effect transistor according to any one of claims 1 to 49, wherein the field effect transistor has a support substrate under said projecting

semiconductor layer, and the semiconductor layer is connected integrally to the support substrate.

51. The field effect transistor according to any one of claims 1 to 49, wherein the field effect transistor has a support substrate under said projecting semiconductor layer, and the semiconductor layer is provided on the support substrate via a buried insulating film.

52. The field effect transistor according to any one of claims 1 to 51, wherein in said channel forming region excepting said channel impurity concentration adjusting region, an electric potential on the side surface of the semiconductor layer increases by 120 mV or more for the n-channel transistor and decreases by 120 mV or more for the p-channel transistor with respect to an electric potential at the central portion of the semiconductor layer.

53. A method for producing the field effect transistor of claim 1 or 2, comprising the steps of:

patterning a semiconductor layer to form a semiconductor layer projecting from the plane of a base;

forming a gate electrode via an insulating film so as to straddle the projecting semiconductor layer; and

ion-implanting a second conductivity type impurity slantingly to the plane of the base from opposite sides of the gate electrode using the gate electrode as a mask to form a channel impurity concentration adjusting region on the upper part of the semiconductor layer under the gate electrode.

54. The method for producing the field effect transistor according to claim 53, wherein in the step of ion-implanting a second conductivity type impurity slantingly to the plane of the base from opposite sides of the gate electrode using the gate electrode as a mask, said ion implantation is carried out at an angle of 10 degrees or less to a plane vertical to the plane of the base and parallel to the longitudinal direction of a channel.

55. The method for producing the field effect transistor according to claim 53, wherein in the step of ion-implanting a second conductivity type impurity slantingly to the plane of the base from opposite sides of the gate electrode using the gate electrode as a mask, said ion implantation is carried out parallel to a plane vertical to the plane of the base and parallel to the longitudinal direction of a channel.

56. A method for producing the field effect transistor of claim 1 or 2, comprising:

a step of patterning a semiconductor layer to form a semiconductor layer projecting from the surface of a base;

a step of forming a gate electrode via an insulating film so as to straddle the projecting semiconductor layer;

a first slanting ion implantation step of ion-implanting a second conductivity type impurity slantingly to the plane of the base from opposite sides of the gate electrode using said gate electrode as a mask; and

a second slanting ion implantation step of ion-implanting the second conductivity type impurity slantingly to the plane of the base from opposite sides of the gate electrode, and at an angle greater than that in said first slanting ion implantation step to a plane vertical to the plane of the base and

parallel to the longitudinal direction of a channel, for each of opposite side surfaces of the semiconductor layer, using said gate electrode as a mask.

57. The method for producing the field effect transistor according to claim 56, wherein said first slanting ion implantation step is carried out at an angle of 10 degrees or less to a plane vertical to the plane of the base and parallel to the longitudinal direction of the channel.

58. The method for producing the field effect transistor according to claim 56, wherein said first slanting ion implantation step is carried out parallel to a plane vertical to the plane of the base and parallel to the longitudinal direction of the channel.

59. A method for producing the field effect transistor of claim 1 or 2, comprising the steps of:

patterning a semiconductor layer to form a semiconductor layer projecting from the plane of a base;

forming a dummy gate electrode so as to straddle the semiconductor layer;

ion-implanting a second conductivity type impurity slantingly to the plane of the base from opposite sides of the dummy gate electrode using said dummy gate electrode as a mask to form a channel impurity concentration adjusting region on the upper part of the semiconductor layer under the dummy gate electrode;

introducing a first conductivity type impurity into the semiconductor layer using said dummy gate electrode as a mask to form source/drain regions;

forming a thick insulating film so as to bury said dummy electrode; and

removing said dummy gate electrode and burying a conductive material in a formed air gap via a gate insulating film to form a gate electrode.

60. A method for producing the field effect transistor of claim 1 or 2, comprising the steps of:

patterning a semiconductor layer to form a semiconductor layer projecting from the plane of a base;

introducing a second conductivity type impurity into the upper part of the projecting semiconductor layer to form said channel impurity concentration adjusting region; and

forming a gate electrode on the side surface of the projecting semiconductor layer via a gate insulating film.

61. A method for producing the field effect transistor of claim 1 or 2, comprising the steps of:

introducing a second conductivity type impurity into a semiconductor layer to form on the upper part of the semiconductor layer a channel impurity concentration adjusting region of which the concentration of the second conductivity type impurity is higher than that in the lower part of the semiconductor layer;

patterning said semiconductor layer to form a semiconductor layer projecting from the plane of a base and having said channel impurity concentration adjusting region for the second conductivity type impurity in the upper part; and

forming a gate electrode on the side surface of the projecting semiconductor layer via a gate insulating film.

62. A method for producing the field effect transistor of claim 20, comprising the steps of:

forming a mask pattern on a semiconductor layer;

ion-implanting a second conductivity type impurity slantingly to the plane of a base from opposite sides of the mask pattern using said mask pattern as a mask to introduce the second conductivity type impurity into the part of the semiconductor layer under the mask pattern in the vicinity of peripheral edge of the mask pattern;

patterning the semiconductor layer using said mask pattern as a mask to form a semiconductor layer projecting from the plane of a base, and having in the upper part first and second channel impurity concentration adjusting regions which are respectively composed of a region of said second conductivity type impurity; and

forming a gate electrode on the side surface of the projecting semiconductor layer via a gate insulating film.

63. A method for producing the field effect transistor of claim 21, comprising the steps of:

patterning a semiconductor layer to form a semiconductor layer projecting from the plane of a base;

forming a gate electrode via an insulating film so as to straddle the projecting semiconductor layer; and

ion-implanting a second conductivity type impurity slantingly to the plane of the base from opposite sides of the gate electrode using said gate electrode as a mask to form first and second channel impurity concentration adjusting regions mutually separated along a pair of sides of the gate electrode on the upper part of the semiconductor layer under the gate electrode.

64. The method for producing the field effect transistor according to claim 63, wherein in the step of ion-implanting a second conductivity type impurity slantingly to the plane of the base from opposite sides of the gate electrode using the gate electrode as a mask, said ion implantation is carried out at an angle of 10 degrees or less to a plane vertical to the plane of the base and parallel to the longitudinal direction of a channel.

65. The method for producing the field effect transistor according to claim 63, wherein in the step of ion-implanting a second conductivity type impurity slantingly to the plane of the base from opposite sides of the gate electrode using the gate electrode as a mask, said ion implantation is carried out parallel to a plane vertical to the plane of the base and parallel to the longitudinal direction of a channel.

66. A method for producing the field effect transistor of claim 23, comprising:

a step of patterning a semiconductor layer to form a semiconductor layer projecting from the plane of a base;

a step of forming a gate electrode via an insulating film so as to straddle the projecting semiconductor layer;

a first slanting ion implantation step of ion-implanting a second conductivity type impurity slantingly to the plane of the base from opposite sides of the gate electrode using said gate electrode as a mask; and

a second slanting ion implantation step of ion-implanting the second conductivity type impurity slantingly to the plane of the base from opposite sides of the gate electrode, and at an angle greater than that in said first slanting ion implantation step to a plane vertical to the plane of the base and

parallel to the longitudinal direction of a channel, for each of opposite side surfaces of the semiconductor layer, using said gate electrode as a mask.

67. The method for producing the field effect transistor according to claim 66, wherein said first slanting ion implantation step is carried out at an angle of 10 degrees or less to a plane vertical to the plane of the base and parallel to the longitudinal direction of the channel.

68. The method for producing the field effect transistor according to claim 66, wherein said first slanting ion implantation step is carried out parallel to a plane vertical to the plane of the base and parallel to the longitudinal direction of the channel.

69. A method for producing the field effect transistor of claim 33, comprising the steps of:

introducing a second conductivity type impurity into a semiconductor layer to form a second conductivity type impurity layer;

epitaxially growing a semiconductor layer having a second conductivity type impurity concentration lower than that of said second conductivity type impurity layer on said semiconductor layer; and

patterning the epitaxially grown semiconductor layer and said second conductivity type impurity layer to form a semiconductor layer projecting from the plane of a base, and having a lower channel impurity concentration adjusting region composed of the second conductivity type impurity layer.